The epHEMT Gate at Microwave Frequencies

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***Abstract*—This paper examines the high-frequency behavior of the enhancement-mode pseudomorphic high electron-mobility transistor (epHEMT) gate. During this study, no bias was applied between the drain and source. Rather, the gate was forward biased with either the drain, source, or channel (drain and source connected together) grounded. While applying positive voltage V_g to the gate, one-port S-parameters were measured from 0.1 to 10 GHz and then converted to Z-parameters. Plotting the real part R of the impedance reveals two sharp peaks. The first peak occurs near the device threshold voltage for conduction in the InGaAs well. A second peak occurs at higher voltages where conduction begins to occur in the surface AlGaAs layer. An equivalent-circuit model is proposed to account for the epHEMT gate's high-frequency behavior and the proposed model is shown to be in good agreement with the experimental data.**

***Index Terms*—Enhancement mode, forward turn-on voltage, gate, heterojunction FET, pseudomorphic.**

I. Introduction

ENHANCEMENT-MODE pseudomorphic high electron-mobility transistors (epHEMTs) are increasingly popular in circuits other than amplifiers. The gate of a high electron-mobility transistor (HEMT) can be used in place of a diode for designing mixers [1], [2], downconverters [3], detectors [4], and voltage-controlled oscillators (VCOs) [5]. To achieve the performance for the application requires a thorough understanding of the gate at high frequency. Measurements of an epHEMT gate have been made to understand the physical mechanisms at RF and microwave frequencies.

To begin, Section II details the epHEMT device, while Section III describes the test setup. Section IV presents dc measurements of the gate forward biased with the channel grounded. The gate's high-frequency impedance (its resistance and capacitance) is discussed in Section V. Proposed in Section VI is an equivalent-circuit model to approximate the epHEMT gate's high-frequency behavior. Section VII summarizes the results.

II. Device Fabrication

The transistor was fabricated using Agilent Technologies' GaAs epHEMT process [6]. The sample device has a gate length of 0.5 μm, a gatewidth of 27 μm, and a drain/source length of 5 μm. Fig. 1 shows a cross section of the epHEMT stack with the dc equivalent-circuit overlaid. Under forward gate bias, two styles of interfaces dominate the gate's electrical performance. The first is a Schottky junction, occurring between the gate metal and the *n* AlGaAs layer. An undoped AlGaAs layer in-between prevents the gate metal from directly contacting the *n* AlGaAs layer, the practical purpose of which is to raise the forward gate turn-on voltage V_F.

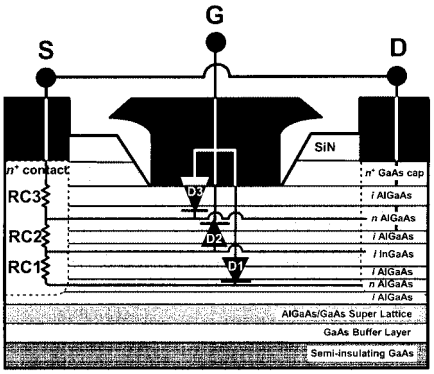

Fig. 1. epHEMT gate (G) overlaid with its dc equivalent circuit. The source (S) and drain (D) are connected together to form a single channel.

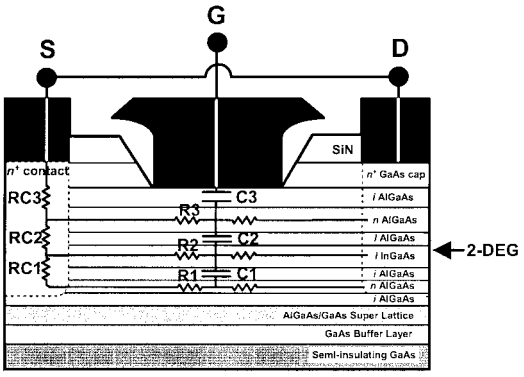

Fig. 2. epHEMT gate overlaid with its high-frequency equivalent circuit. The width of the gate is exaggerated to show the locations of the circuit elements.

The second style interface is a hetero-interface across both the *i* AlGaAs and the *i* InGaAs. In normal epHEMT action, a two-dimensional electron gas [(2-DEG), as indicated in Fig. 2] is formed within the intrinsic InGaAs channel. Depending on the gate voltage V_g, donors to the channel come from the *n* AlGaAs layers above and below the *i* AlGaAs layer.

III. Test Setup

Agilent-EESof's IC-CAP software was used for high-frequency characterization of the epHEMT gate. IC-CAP enables simple control of the Agilent 8510C vector network analyzer (VNA) and 4142B dc power supply. Agilent 11612T bias tees were especially helpful, having force and sense triaxial connections to the 4142B. This arrangement permits current measurement resolution in the sub-picoampere range. The

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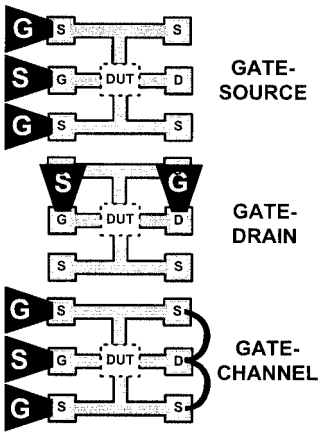

Fig. 3. epHEMT die are probed in three configurations using either G–S–G or G–S coplanar probes. At bottom, the source (S) and drain (D) are connected with bond wires to form a single channel.

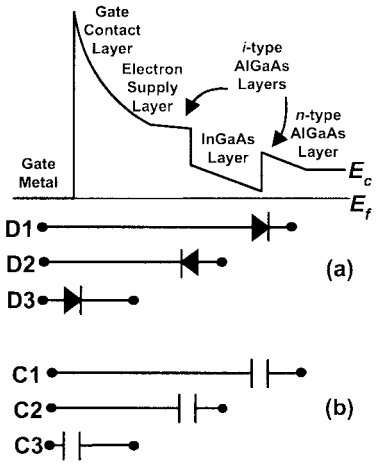

Fig. 4. Energy band diagram of the epHEMT with no bias applied. Shown below are: (a) dc and (b) high-frequency circuit elements corresponding to each interface.

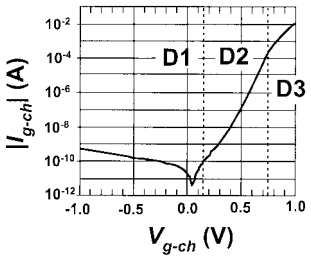

Fig. 5. Current–voltage (I–V) measurement of the epHEMT in gate–channel configuration.

wafers were loaded onto a Cascade Microtech Model 41 probe station. The wafer chuck was manually moved from die to die.

Fig. 3 shows the three configurations for studying the gate. To measure from gate to source (G–S), a ground–signal–ground (G–S–G) coplanar probe contacts the source (S) and gate (G) pads while the drain (D) is left floating. To probe from gate to drain, a signal-ground coplanar probe contacts across the epHEMT device with the source unconnected. For the gate-to-channel (G–Ch) case, a G–S–G coplanar probe contacts the source and gate pads, while bond wires connect the drain and source pads together on the opposite side. The coplanar probes were calibrated using a Cascade Microtech impedance standard substrate (ISS) designed for either balanced (G–S–G) or unbalanced (signal–ground), depending on the probes. Calibration coefficients corresponding to each ISS were entered into the 8510C.

With the drain and source connected together, the gate current is uniformly distributed throughout the channel at dc. However, bond-wire inductance leads to a slight voltage drop at high frequencies and high currents, resulting in a slightly lower potential on the drain. At the frequencies ($\leq$ 10 GHz) and currents ($\leq$ 10 mA) measured in this study, the potential drop is not believed to have a significant impact.

IV. dc Performance

Shown in Fig. 4 is an energy band diagram for the epHEMT. In our case, a positive voltage V_g is applied to the gate with the channel grounded. At dc, the gate current is roughly divided between the source and drain paths, although the source is slightly closer than the drain to the gate. The gate current is dominated by three mechanisms, the metal-to-*n* AlGaAs Schottky interface diode (D3), the AlGaAs–InGaAs hetero-interface diode (D2), and the InGaAs–AlGaAs hetero-interface diode (D1) [7]. When initially applying V_g, the first to conduct is D1. The D1 conduction path is along the edge of the gate finger, vertically down through to the *n* AlGaAs layer below the *i* AlGaAs layer, traveling laterally along the *n* AlGaAs to the contact resistor RC1. For V_g above the threshold voltage $V_{\rm th}$, the entire area underneath the gate finger conducts [8]. According to conventional circuit theory, V_g should be dropped entirely across the reverse-biased diode D2. Yet the Schottky barrier height of D3 is approximately four times larger than the barrier heights of either D1 or D2, so that the saturation current $I_{\rm sat3}$ across D3 is much smaller than $I_{\rm sat}$ across either D1 or D2 [9]. That is to say, the resistance across D3 is much larger than either D1 or D2 so that D3 does not contribute significant current flow below $V_{\rm th}$. Above $V_{\rm th}$, applied V_g drops primarily across D2 and D3, with a significant amount dropping across D3 [10], [11]. Above the forward turn-on voltage V_F, V_g is dropped almost solely across D3. For the sake of brevity, this analysis does not detail quasi-Fermi level bending as V_g increases [12].

Fig. 5 shows the magnitude of the dc current flowing through the gate to the channel. In an epHEMT, the gate is normally operated under forward bias. Not apparent from the plot in Fig. 5 is the direction of current flow. From -1 V to 50 mV, the current flow I is negative with I flowing into the gate from the channel. Above 50 mV, the current changes direction and flows positively into the channel from the gate. Distinct inflection points in the slope are seen at 50, 150, and 750 mV. To fit to a traditional diode model, each segment between inflection points requires its own unique ideality factor n. At low $V_{\rm g-ch}$, typical values are $n > 1.3$, while at high $V_{\rm g-ch}$, they can be $n > 6$.

V. High-Frequency Performance

One-port S-parameter measurements were made at 100 MHz, 2 GHz, and 10 GHz and then converted into one-port Z-parameters. The frequencies were chosen high enough to avoid phenomena such as surface states and traps [13]. Fig. 6 shows a

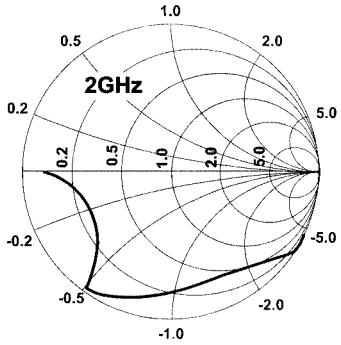

Fig. 6. One-port S-parameter plot versus G–Ch voltage ($V_{\mathrm{g-ch}}$) at a single measurement frequency.

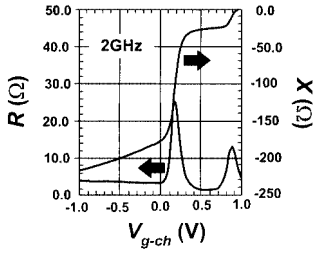

Fig. 7. Real (R) and imaginary (X) parts of the epHEMT gate impedance versus G–Ch voltage ($V_{\mathrm{g-ch}}$) measured at 2 GHz.

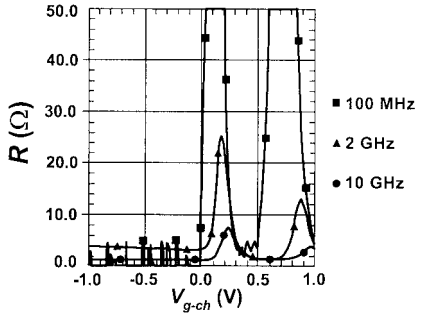

Fig. 8. Real (R) part of the epHEMT gate impedance versus G–Ch voltage ($V_{\mathrm{g-ch}}$) measured at 100 MHz, 2 GHz, and 10 GHz.

2-GHz Smith chart plot of a one-port G–Ch S-parameter measurement. The measurement is converted to Z-parameters in Fig. 7. Sweeping the G–Ch voltage $V_{\mathrm{g-ch}}$ from -1 V to $+1$ V, the real R and imaginary X parts are plotted on separate axes. The imaginary part X resembles capacitance curves found elsewhere in the literature [14], [15]. It is the plot of the real part R that shows unique behavior. It has two sharp peaks, each centered around a major transition region of X.

Fig. 8 shows R versus $V_{\mathrm{g-ch}}$ at three discrete frequencies. As the frequency increases, the magnitude of R gets smaller and the peaks shift slightly toward higher $V_{\mathrm{g-ch}}$. Similar behavior was recorded for the gate–source (Fig. 9) and gate–drain (Fig. 10) configurations. At 100 MHz, the peaks in R roughly coincide with inflection points in the I–V curve of Fig. 5.

The epHEMT gate capacitance has three components, i.e., the vertical sidewall depletion capacitance into the *n* AlGaAs layer, the capacitance between the gate metal and the carriers in the 2-DEG layer, and the sidewall capacitance from the gate metal to the drain and source metals [16]. A threshold voltage $V_{\mathrm{th}} > 0$ V is desirable to avoid source-to-drain leakage current.

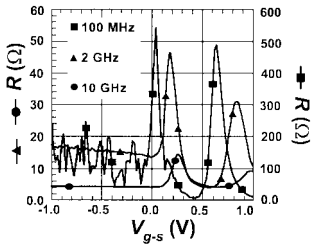

Fig. 9. Real (R) part of the epHEMT gate impedance versus gate–source voltage ($V_{\mathrm{g-s}}$) measured at 100 MHz, 2 GHz, and 10 GHz.

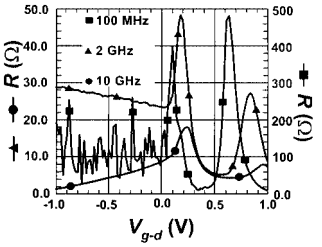

Fig. 10. Real (R) part of the epHEMT gate impedance versus gate–drain voltage ($V_{\mathrm{g-d}}$) measured at 100 MHz, 2 GHz, and 10 GHz.

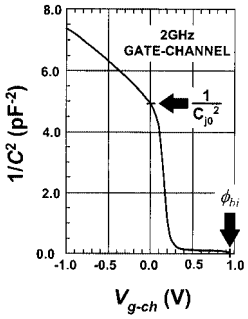

Fig. 11. Plot of the capacitance $1/C^2$. With this curve, the junction capacitance at 0 V C_{j0} and the built-in potential ϕ_{bi} can be found graphically.

Per Fig. 5, $V_{\mathrm{th}} = 150$ mV. Above V_{th}, the *n* AlGaAs layer begins to donate electrons to the 2-DEG. The electron flow to the 2-DEG increases exponentially just below V_{th}, linearly just above V_{th}, and exponentially well above V_{th} [17], [18].

Using X from Fig. 7, the gate capacitance versus G–Ch voltage $V_{\mathrm{g-ch}}$ is shown in Fig. 11. Plotting the capacitance as $1/C^2$ reveals a linear region for negative voltages below threshold indicating a uniform substrate doping [19], [20]. Around and above the threshold voltage, the $1/C^2$ curve drops rapidly as the conducting channel forms.

Fig. 12 illustrates how the electrons overcome the energy barriers with forward-bias V_g [5]. While the dc current is controlled by the diode resistances, at high frequencies, the capacitances of the various layers (as illustrated in Fig. 2) become important. These are really distributed resistance–capacitance effects along the length of the gate since current through the gate must flow laterally through the resistances to reach the source/drain contacts [21], [22]. A first-order model is shown in Fig. 2 with lumped resistances and capacitors as C_1, C_2, C_3, R_1, R_2, and R_3. Resistance R_1 represents the substrate resistance, while R_2 and R_3 represent the resistance of the InGaAs channel and top surface AlGaAs layer, respectively. These latter two resistances are strong functions of the dc operating point.

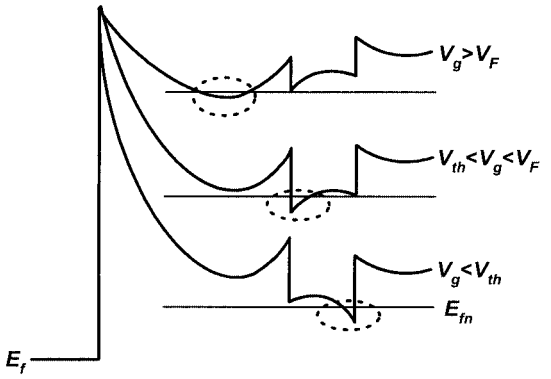

Fig. 12. Band diagram of the epHEMT at three different gate voltages. The dotted circles show where electrons accumulate. Below threshold ($V_g < V_{\rm th}$), minor conduction occurs in the lower *n* AlGaAs layer where the conduction band dips slightly below the quasi-Fermi level E_{fn}. Between threshold and turn-on ($V_{\rm th} < V_g < V_F$), conduction occurs principally through the 2-DEG. At voltages above turn-on ($V_g > V_F$), the *n* AlGaAs supply layer dips below E_{fn} and conduction transfers from the InGaAs 2-DEG to the *n* AlGaAs layer.

With reference to Fig. 2 and the energy band diagrams in Fig. 12, a general discussion of the high-frequency currents as a function of bias voltage can be given. At negative voltages, the structure is essentially fully depleted of conduction electrons and the depletion region extends to the back surface *n* AlGaAs layer. Current flow is essentially through the series combination of C_3, C_2, C_1 (Fig. 2), and through the substrate resistance represented by R_1 and out through the n^+ contact resistances. In this voltage region, the resistances R_2 and R_3 of Fig. 2 have large values and do not enter into the operation. The measured reactance (Figs. 6 and 7) is large and negative, indicating a small capacitance in series with a resistance of approximately 4 Ω. The increased negative impedance seen with increasing negative bias is due to the increasing depth of the depletion layer with bias voltage into the substrate. At a slightly positive gate voltage of around 0.1 – 0.15 V, as seen in Fig. 7, the magnitude of the reactance decreases rapidly as the capacitance increases. This occurs around the epHEMT device threshold voltage where Fig. 12 indicates mobile carriers are accumulating in the InGaAs channel layer. In this region of gate voltage, the channel resistance of R_2 in Fig. 2 is a strong function of gate voltage. As R_2 decreases in value, the high-frequency current switches from flowing through $C_1 + C_2 + C_3$ and R_1 in series to eventually flowing through $C_2 + C_3$ and R_2 in series. The plateau in reactance from Fig. 7 indicates that at approximately 0.5 V positive on the gate, the transition to $C_2 + C_3$ is essentially complete and the series resistance is again at approximately 2 Ω. The peak in measured resistance at around 0.2 V is a consequence of the switching of current flow into the $C_2 + C_3$ and R_2 combination coupled with the voltage dependence of R_2. A model is subsequently presented to verify that this is the correct explanation of the resistance peak.

The second peak in measured high-frequency resistance seen in Fig. 7 at around 0.9-V gate bias occurs in combination with another decrease in reactance to a very small negative value. This is due to the accumulation of electrons in the top surface AlGaAs layer, as illustrated in Fig. 12 for $V_g > V_F$. The ac current flow eventually approaches the series combination of C_3 and R_3 as the resistance R_3 decreases due to the electron accumulation in the top AlGaAs layer.

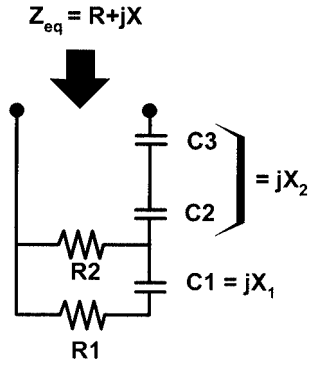

Fig. 13. Model of high-frequency effects at negative and small forward voltages.

This provides a general explanation of the measured ac parameters. Section VI presents a more detailed first-order modeling of the effects to help verify the proposed model.

VI. Model of High-Frequency Effects

For negative voltages and small forward bias gate voltages, a proposed model of the high-frequency effects is given in Fig. 13. For simplicity in this model, the contact resistances ($R_{C1} - R_{C3}$) of Fig. 2 are neglected. An analysis of the equivalent circuit gives for the equivalent resistance and reactance at the terminals

$$R = R_2 \frac{R_1(R_1 + R_2) + X_1^2}{(R_1 + R_2)^2 + X_1^2} \tag{1}$$

$$X = X_2 + X_1 \frac{R_2^2}{(R_1 + R_2)^2 + X_1^2}. \tag{2}$$

From the experimental measurements in Fig. 7, values of many of the parameters can be determined. For large negative gate voltages, where $R_2 \to \infty$, one can estimate that $R_1 = 4\ \Omega$ and $X_1 + X_2 = -175\ \Omega$ at 0-V bias and increases to $X_1 + X_2 = -230\ \Omega$ at −1.0-V bias.

From the plateau region in X at around 0.5–0.7 V, one can estimate that $X_2 = -25\ \Omega$ and $R_2 = 2\ \Omega$ at $V_g = 0.55$ V. The impedance X_1 has a voltage dependence, which can be modeled from the data in Fig. 7, and the measured capacitance data, as seen in Fig. 11. In the negative-bias region, $1/C^2$ has an approximate linear relationship suggesting a relationship of the form $X_1 = X_{10}\sqrt{1. - V_g/V_{\rm bi}}$. The values in Fig. 7 give $X_{10} = -150\ \Omega$, $V_{\rm bi} = 1.45$ V when a constant value of $X_2 = -25\ \Omega$ is used for the 0.5 – 0.7-V range. Taking R_1 as constant at approximately 4 Ω leaves only the voltage dependence of R_2 to be modeled.

R_2 is assumed to be the channel resistance of the FET, which sufficiently above the threshold voltage should be given by an equation of the form

$$R_2 \to \frac{K}{(V_g - V_{\rm th})} \tag{3}$$

where $V_{\rm th}$ is the device threshold voltage $= 0.15$ V. A match to the measured resistance of approximatley 2 Ω at 0.55 V would

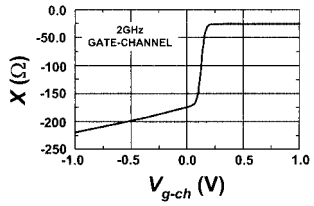

Fig. 14. Modeled imaginary (X) part of the epHEMT gate impedance versus G–Ch voltage ($V_{\mathrm{g-ch}}$) at 2 GHz.

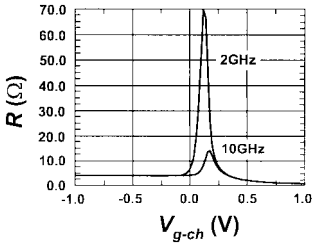

Fig. 15. Modeled real (R) part of the epHEMT gate impedance versus G–Ch voltage ($V_{\mathrm{g-ch}}$) at 2 GHz and 10 GHz.

give $R_2 = 2\,\Omega\,[0.4\,\mathrm{V}/V_g - V_{\mathrm{th}}]$. This simple model would predict an infinite resistance at $V_g = V_{\mathrm{th}}$, and we know this is not the case, but that the channel carrier density only exponentially approaches zero near and below the threshold voltage. This can be modeled in terms of resistance as

$$R_2 = R_0 \exp\left[-\frac{q(V_g - V_{\mathrm{th}})}{nkT}\right] \tag{4}$$

where n accounts for the fact that not all the applied voltage is dropped across the channel giving rise to the conductance. In standard terms, n can be related to the capacitances and reactance as

$$n = \frac{C_1 + C_{23}}{C_{23}} = \frac{X_1 + X_2}{X_1} \tag{5}$$

where C_{23} represents C_2 in series with C_3. In the region around threshold (near 0 V), $n = 1.17$.

A typical way of joining together the approximations of (3) and (4) is to join them so that both the value and first derivative of R_2 are continuous. When this is done, one obtains (6) as follows:

$$R_2 = \begin{cases} (2\,\Omega)\dfrac{(0.4\,\mathrm{V})}{(V_g - V_{\mathrm{th}})}, & \text{for } V_g \geq V_{\mathrm{th}} + \dfrac{nkT}{q} \\ (2\,\Omega)\left(\dfrac{0.4\,\mathrm{V}}{\left(\frac{nkT}{q}\right)}\right)\exp\left[1. - \dfrac{q(V_g - V_{\mathrm{th}})}{nkT}\right], & \text{for } V_g \leq V_{\mathrm{th}} + \frac{nkT}{q}. \end{cases} \tag{6}$$

With these values, the model is complete and the equivalent resistance and reactance of (1) and (2) can be evaluated.

The resulting calculations are shown in Figs. 14 and 15 for the modeled reactance and resistance, respectively. First consider the calculated equivalent resistance in Fig. 15 compared with the measured experimental values shown in Fig. 8. The calculated values show the same general trends seen in the experimental data. The peak resistance is a strong function of frequency and the gate voltage at which the peak occurs shifts to larger values with increasing frequency. However, the calculated peak values are approximately a factor of two larger than the measured peak values.

The calculated reactance transitions shown in Fig. 14 can be compared with the experimental transition shown in Fig. 7. Again, the general trends are correct with the reactance plateau around 0.5 V and the rapid transition in reactance around the threshold voltage. However, the calculated transition in reactance and, hence, capacitance from the deep depletion capacitance to the channel capacitance is too abrupt as compared with the experimental transition. This is due to the fact that the G–Ch capacitance model used in the calculation is a little too simple. The G–Ch capacitance $C_2 + C_3$ is assumed to be a constant. In fact, as illustrated in Fig. 12, as carriers are first added to the channel, they are added near the back side of the channel and, as the channel becomes filled with carriers, they are added near the top side of the channel. This effect will cause a slower increase in G–Ch capacitance than included in the model calculations used here.

This slower change in capacitance or in reactance will also cause the peak equivalent resistance of the modeled circuit to decrease. This is believed to be the major cause of the modeled resistance being approximately a factor $2\times$ larger than the experimental values. However, the difference could also be due to a somewhat lower channel resistance than that of the approximate model used here. The good agreement in the general trends observed is considered sufficient to verify the proposed model for the observed peaks in the measured terminal resistance at high frequencies.

The second peak in resistance seen in the data of Fig. 7 at around 0.9 V coincides with another capacitance transition as the surface AlGaAs layer begins to accumulate electrons. As electrons accumulate in the AlGaAs layer closer to the surface, the high-frequency capacitance shows a transition to a larger capacitance value (lower X value) representing the capacitance between the gate and the potential minimum in the AlGaAs layer. The electron layer in the AlGaAs layer also presents a new conduction path to the source and drain contacts, which is voltage dependent. This peak in equivalent terminal resistance is again believed to be due to the current flow making a transition in Fig. 2 from flowing through $C_2 + C_3$ in series with R_2 to a flow through C_3 alone in series with R_3, where R_3 is the resistance of the electron layer in the AlGaAs layer. A model for this transition would be similar to that already studied in (1) and (2), but with different parameters (i.e., C_3 in place of $C_2 + C_3$ and R_3 in place of R_2) and will not be developed here.

VII. Summary

This paper has detailed the high-frequency behavior of the gate of an epHEMT, modeled as diodes at dc and distributed capacitors and resistors at high frequency. Two high-frequency resistance peaks coincide with the transition regions of the imaginary part X. Expressions suitable for an equivalent-circuit model are shown to approximate the epHEMT gate's measured impedance.

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